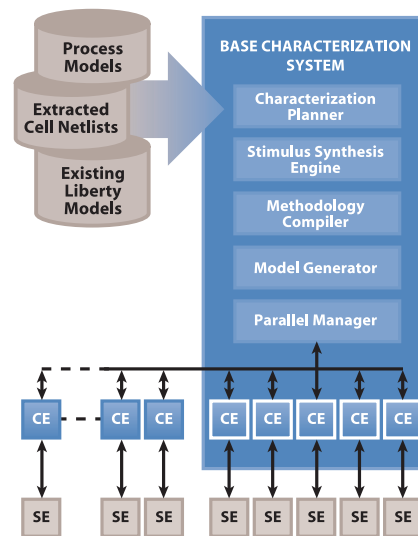


SiliconSmart[®] and SiliconSmart HP

- Adaptive parallel job manager provides the fastest throughput and is fully scalable to take advantage of an unlimited number of CPUs, delivering unrivalled performance utilizing the highest level of parallelism (on an arc-by-arc basis).
- Intelligent characterization planning further optimizes runtime without sacrificing industry leading accuracy.
- Traditional non-linear delay and power models for 90-nm and higher designs.
- IBIS models for I/O cells are fully supported.
- Fast turnaround of library models for new process model updates, custom PVTs, or custom cells enabled through the re-characterization flow.
- Automated characterization setup for complex standard cells and I/Os eases adoption.
- Advanced constraint acquisition methodologies for maximum setup/hold requirement accuracy.
- Verilog and Vital/VHDL models consistent with SDF are generated from Liberty models to enable gate level simulations.
- Platform for SiliconSmart Sign-Off and DFM Extensions.
- Accurate models to eliminate silicon re-spins.
- Supports a wide variety of both industry-standard and customer-proprietary simulators.
- Models easily integrate with all popular design flows.
- Automatic stimulus creation, characterization and modeling setup provide ease of use and low cost of ownership.

Featuring industry leading accuracy, throughput and ease of use, SiliconSmart provides standard cell and I/O characterization and modeling for all popular design flows and supports advanced timing and power modeling. It is a complete library characterization and publishing system that produces production-ready models with minimal setup effort. For maximum performance, SiliconSmart HP (High Performance) embeds Magma's high-speed SPICE simulator, FineSim™ SPICE, providing a 2x improvement in throughput. Both are backed by dependable worldwide customer support and provide the most reliable and shortest path to high-quality, production-ready nanometer models.

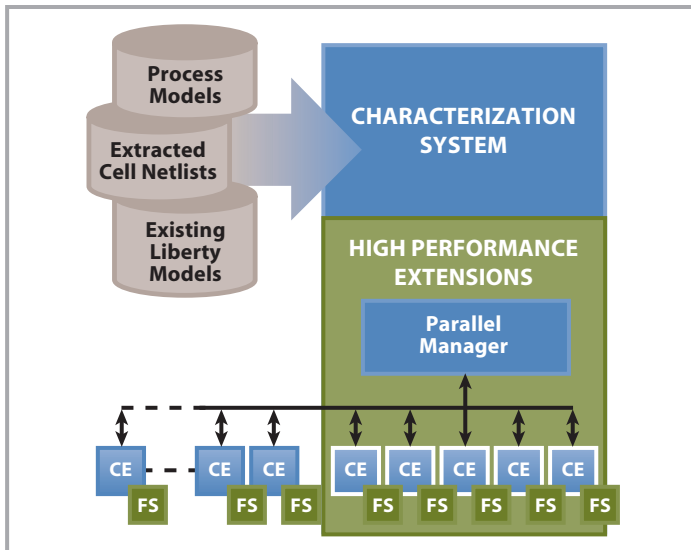


Library developers, IP vendors and COT design teams rely on abstract models to accurately represent the electrical behavior of circuits implemented with advanced process technologies. To meet the needs of these customers, the SiliconSmart product suite characterizes standard cells, I/O cells and embedded memories to provide robust timing (including current source models), low-power, signal integrity and design for manufacturability (DFM) models in a variety of industry standard formats. Unlike other solutions, SiliconSmart combines accuracy, throughput, comprehensive standard-format support, ease of use and highly experienced worldwide support in one product. When used with popular construction and verification tools, these models offer silicon predictability and improved designer productivity. As a result, SiliconSmart models help customers shorten design cycles and improve chip performance.

SiliconSmart® and SiliconSmart HP

SiliconSmart HP

To provide a 2x throughput improvement over the industry leading performance of the base SiliconSmart system, Magma has embedded its high-speed FineSim SPICE simulator in the SiliconSmart HP product. This eliminates the need to start and stop the simulator or reload process models and allows the use of the highly efficient characterization algorithms in FineSim SPICE. SiliconSmart HP includes all the features of the base product, including industry standard accuracy and remarkable ease of use for standard cell and I/O characterization, modeling for all popular design flows, and advanced timing and power modeling.



SiliconSmart Sign-Off and DFM Extensions

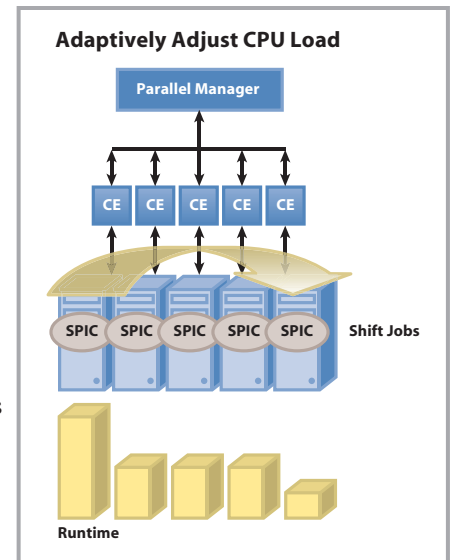
SiliconSmart and SiliconSmart HP provide fundamental library characterization features and capabilities. Additional extensions are also available that target specific design challenges, including sign-off and design for manufacturability (DFM).

Sign-off Extensions enable advanced modeling constructs that allow the timing, power and noise analysis and repair flows that are required at 90-nanometers (nms) and below. They include support for the latest modeling formats such as composite current source (CCS) and effective current source model (ECSM) for timing, power and noise. These models enable transient current modeling for standard cells, power switch cells and MTCMOS cells, allowing validation of the integrity of the power and ground network for low-power chips.

SiliconSmart DFM Extensions generate statistical and sensitivity models for timing and leakage. DFM characterization identifies cells prone to performance degradation due to lithographic (systematic) or process (random) variation, enabling optimization for better yields at higher frequencies.

Throughput Maximization

SiliconSmart and SiliconSmart HP intelligently combine measurements into simulations, optimizing the number of simulations and accelerating that process. The adaptive job manager then distributes simulations to as many CPUs and simulator licenses as are available, and automatically adjusts CPU loads based on



CPU performance. Overall characterization throughput improvements are nearly linear with each additional CPU. As a result SiliconSmart and SiliconSmart HP are able to significantly speed up characterization runtime.

The data dependency manager feature eliminates the need to re-characterize an entire library or cell by immediately identifying which cells are affected by changes to the transistor netlist or technology process settings. This can result in a huge runtime savings in the generation of accurate and production-ready library models.

Techniques to reduce simulation runtime include sharing state-specific characterization (known as state binning), netlist pruning and sequential cell path recognition to reduce the number of simulations required for setup/hold constraint measurements. These are determined during pre-characterization which is a fast, low-resolution simulation performed in order to speed-up the characterization runtime.

Automated Characterization Setup for Complex Functions

Stimulus creation, characterization and modeling are largely automated for complex functions and I/Os in addition to normal standard cells. SiliconSmart and SiliconSmart HP use complex state table definitions of functional behavior for deriving the required stimulus as well as structural descriptions. This allows the composition of a block-level description of the cell. Differential inputs and outputs, user-specifiable complex load networks and variable electrical modes are all supported.

Ease of Use – Low Cost of Ownership

The stimulus creation, characterization and modeling setup is largely automatic with default settings available for all required parameters. This saves a significant amount of time and eases adoption.

All major industry standard and customer proprietary circuit simulators are supported for characterization. Support for additional simulators is constantly being added on the basis of customer need.

SiliconSmart and SiliconSmart HP users also have access to a highly professional, worldwide team of application engineers to resolve software issues.

Industry Leading Accuracy for Timing and Power

SiliconSmart and SiliconSmart HP determine the maximum load needed for characterization by automatically deriving this data from the maximum output slew setting in the library during pre-characterization. The tool also determines realistic waveform shapes for the input stimulus used for characterization by employing actual driver cells or emulated models (complex piecewise linear or nonlinear waveforms).

Silicon Smart supports a wide range of constraint methodologies, from standard design flows to bleeding-edge performance applications for maximizing yield and performance. For example, SiliconSmart provides multiple ways of capturing the dependency between setup and hold checks. Considered independently, these two checks can result in a negative pulse where data is not allowed to change – something that is not possible in the same cycle. Thus, the dependency needs to be considered to the degree that is appropriate for your design style.

SiliconSmart also allows sampling of internal nodes in a flip-flop to look for glitches in order to remove potential optimism for setup/hold constraints.

Customization and Accuracy Control in Power Characterization

At 90 nm or below, leakage power starts to dominate, making internal switching power measurement difficult. Subtracting leakage power and output capacitance switching power can lead to negative numbers for internal switching power. Magma's methodology guidance and advanced characterization algorithms make it easier to interpret negative values and set up your characterization with the best accuracy and runtime combination. SiliconSmart and SiliconSmart HP properly account for leakage power, external switching power, hidden power (internal switching power when output values do not transition in response to an input transition), multiple output cells and multiple power rail cells to meet the needs of various power analysis and optimization tools.

Adding Capacity

The parallel manager can support an unlimited number of CPUs in the network to maximize throughput. The default configurations for SiliconSmart and SiliconSmart HP support 5 CPUs (with FineSim SPICE for the HP system). Additional CPUs can be supported by adding a characterization engine

(along with FineSim SPICE for the HP system) for every additional CPU desired.

TECHNICAL FEATURES

- Tcl command line user interface
- Distributed processing on heterogeneous compute farms with unlimited CPU counts
- Support for industry-standard load sharing systems
- Automatic library setup
 - Automatic stimulus creation for cell functions read in from Liberty files including complex state table-based functions
 - Automatic characterization deck setup including determining the slew and load indices
 - Automatic gathering of all data from simulation runs for characterization to create Liberty files for timing and power
- State- and path-dependent timing and power
- Extremely accurate power characterization methods designed for nanometer processes
- Dependency management

Cell Types

- Single- and multi-output combinatorial cells
- Complex latches and flip-flops
- Electrically complex multi-voltage, bi-directional I/O cells
- Tri-state and open drain cells
- Special cells (one-hot MUX, bus keeper, etc.)

I/O Features

- Differential inputs and outputs
- Multiple voltage supplies
- User specifiable complex load networks
- Characterization of multiple electric modes per driver

Measurements

- Intrinsic delay and output transition time
- Effective input pin capacitance
- Minimum pulse widths
- Setup, hold, recovery and removal times
- Constraint edge control
 - Independent setup and hold
 - Dependent setup and hold
- Constraint violation determination
 - Functional failure
 - Absolute, relative and user-defined delay or slew degradation
 - Output and internal node glitch checking
- Leakage and internal (transition and hidden) power
- IBIS 4.1 measurements including current and voltage curves plus differential launch delay

Model Views

- Liberty (.lib)
- Verilog
- VHDL/Vital
- IBIS 4.1 I/O models

Platform Support

- Sun Solaris
- Linux (Red Hat)

Supported SPICE Simulators

- FineSim™ SPICE
- FineSim Pro
- HSPICE
- Spectre

MAGMA DESIGN AUTOMATION

SiliconSmart® and SiliconSmart HP



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