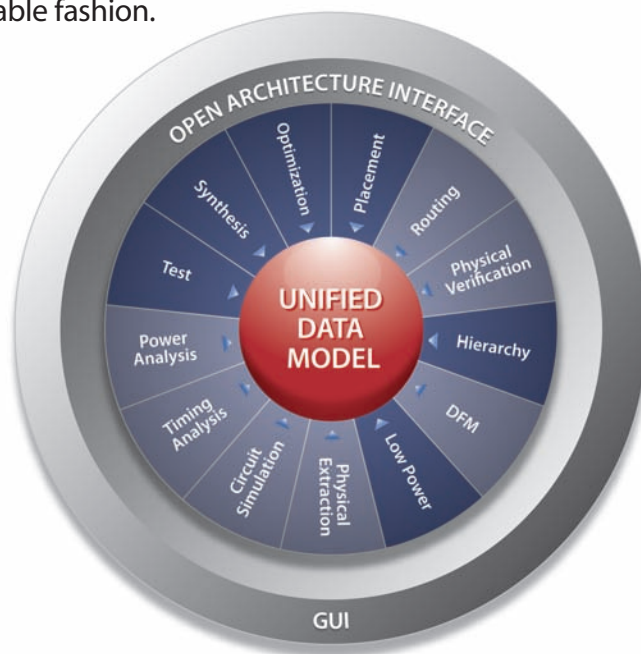


# Talus<sup>®</sup> Design

- Full-featured RTL, DFT and data-path synthesis for smaller area, higher performance and lower power.
- Fully automated macro placer flow with underlying RTL synthesis and optimization technology enables rapid exploration of the design space with handoff to the physical implementation flow, and provides a predictable path to design closure.
- Timing and congestion-driven macro legalization removes need for block-level floorplanning.
- Early RTL, DFT and netlist checks result in accelerated problem detection and correction, rapidly improving the quality of input.
- Significant improvement in ROI achieved through 30 percent reduction in turnaround time and 20 percent reduction in development cost.
- Very large capacity and fast run times allow complexity scaling without compromising productivity, requiring additional engineering resources or adversely affecting schedules.

Talus Design is a full-chip synthesis environment that enables rapid development of RTL and chip-level constraints throughout the design process without sacrificing the quality of design or delivery schedule. This integrated environment dramatically improves the productivity of chip architects and logic designers by automating data-path synthesis and floorplan generation for prototyping. Talus Design and Talus Vortex together enable any size design to be implemented from RTL to GDSII in a predictable fashion.



Design engineers must make changes in the design specification throughout the implementation phase. In traditional hierarchical flows, once the RTL, timing and physical constraints are incorporated, substantial manual effort is required to propagate changes into the hierarchy, floorplan, size and shape of physical partitions and pad locations. For System-on-Chip (SoC) designs at 65 nanometers (nm) and below, designers need an automated top-down or bottom-up full-chip synthesis methodology. Talus Design, in conjunction with Hydra™, addresses all aspects of the design flow, eliminates time-consuming manual work, prevents the introduction of new errors – especially for changes that must be made late in the design phase – and ensures design closure.

Talus Design includes production-proven RTL synthesis, automated macro placement capabilities and physical synthesis, and a timing analyzer. Talus Design synthesizes full-chip RTL for given timing, power and placement constraints. This automated solution empowers logic designers to rapidly explore the design space and implement the optimum solution without detailed knowledge of physical design and without sacrificing the schedule or quality of the design. Built on Magma's unified data model architecture, Talus Design provides logic designers with an integrated, highly productive, predictable and repeatable flow.

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## Fast, High-Capacity RTL, DFT and Data-Path Synthesis

Leveraging the high capacity of Magma's unified data model, Talus Design synthesizes several-million-gate RTL designs without hierarchical partitioning or guard-banding-related timing constraints. Synthesizing the entire chip or very large

```
typedef enum logic [1:0] {xst[4]} xmit_state ;
typedef enum {ON, OFF, WAITING} det_state ;

xmit_state base_xst, base_xst_n ;
det_state d_unit ;

always_ff @(posedge xmit_clock iff xmit_rst ==1
           or negedge xmit_rst)
begin
  if (!reset) base_xst <= xst[0] ;
  else base_xst <= base_xst_n ;
end

always_comb
begin
  d_unit = WAITING ;
  xcnt += pkt_cnt ;
  case (base_xst)
```

*Automated flow starts from RTL synthesis.*

logic partition, instead of numerous submodules, produces superior optimization results because the flow is not limited by arbitrary boundaries. An incremental elaboration capability allows small changes to the design's RTL to be propagated quickly into the implementation flow without the time-consuming and error-prone manual process of recompiling the entire design.

Talus Design includes a built-in dynamic arithmetic module generator that infers data-path elements within the RTL source and considers timing constraints to automatically implement the best micro-architecture that achieves required performance while minimizing area and power. Unlike traditional synthesis, Magma's module generator globally synthesizes entire arithmetic expressions using operator merging and by sharing common operations across hierarchical boundaries to generate the best architecture for the entire data-path module. Taking advantage of its fast synthesis capability, Talus Design implements data-path modules dynamically, without creating large caches of alternative architectures. Talus Design also has the unique ability to swap architectures during physical synthesis to achieve the desired performance.

To ease adoption of this powerful, automated design environment, Talus Design synthesizes and optimizes RTL input in all of the industry-standard HDL formats, including System Verilog (IEEE 1800), Verilog (IEEE 1364-1995 and 1364-2001) and VHDL (IEEE 1076-1987, 1076-1993). Talus Design is compatible with widely used coding styles for synthesis and reuse. Talus Design also supports synthesis pragmas and instantiated arithmetic data-path components used in legacy commercial synthesis tools.

## Strength-Based Delay Model for Optimal Timing

With Talus Design, Magma introduces optimization capabilities based on the new strength-based delay model. This new delay model accurately considers the effects of buffering and sizing at an early stage of optimization. Each cell is assigned a continuous drive strength that abstracts actual size available in the technology

library. Rather than using fixed cells from a library, Talus Design replaces each logic function with automatically abstracted HyperCell™ models. These are functional placeholder cells with variable drive strength.

Initial placement and routing is done with the HyperCell model to determine the final optimal timing for all paths in the design. Layout optimization is performed by continuously adjusting the strength of each HyperCell as load and timing changes throughout the optimization process, allowing optimal delay to be achieved at any stage of optimization. Finally, the HyperCells are mapped to actual library cells with a discrete size. By employing optimal continuous sizing combined with adaptive buffering, Talus Design is able to deliver designs that consume less power and area while meeting timing requirements.

## Built-in Low-Power Design and Optimization

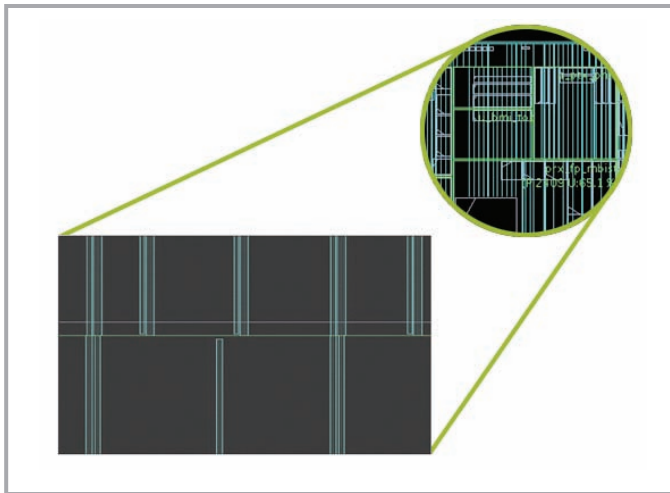
Talus Design provides an integrated power optimization flow, reducing power up to 20 percent over conventional standalone synthesis tools while also delivering high performance. Power optimization capabilities deliver lower dynamic power consumption than conventional synthesis. Only optimal cell sizes are used to drive known loads, avoiding unnecessary power dissipation by cells. Balancing input slews to cells through optimal sizing is used to reduce total switching power. Additional power optimization capabilities such as multi-Vt library-based optimization, DFT-aware automatic clock gating, use of integrated clock-gating cells in standard-cell library, detection of synchronously enabled registers and hierarchical insertion of clock-gating logic minimize power and improve testability.

Utilizing automatic power-grid synthesis for optimal power distribution, Talus Design, with Talus Power as an option, accepts user-defined power-grid constraints and automatically generates the appropriate power mesh. This method is extremely efficient in comparison to the spreadsheet approach that approximates power numbers based on legacy designs. Users can define utilization limits for each layer, current density or the voltage-drop limit as input constraints. Designers can also specify optimal parameters for the power grid and define pad locations during early planning, and then continue the refinement during detailed implementation. This eliminates the need to overdesign the power grid, saving precious routing resources and real estate on the chip. This automated method significantly reduces design closure time without sacrificing performance.

Advanced, low-power design capabilities are available as an option. These include voltage island support, automatic MTCMOS switch insertion, and Unified Power Format (UPF).

## Automated Macro Placement and Physical Synthesis

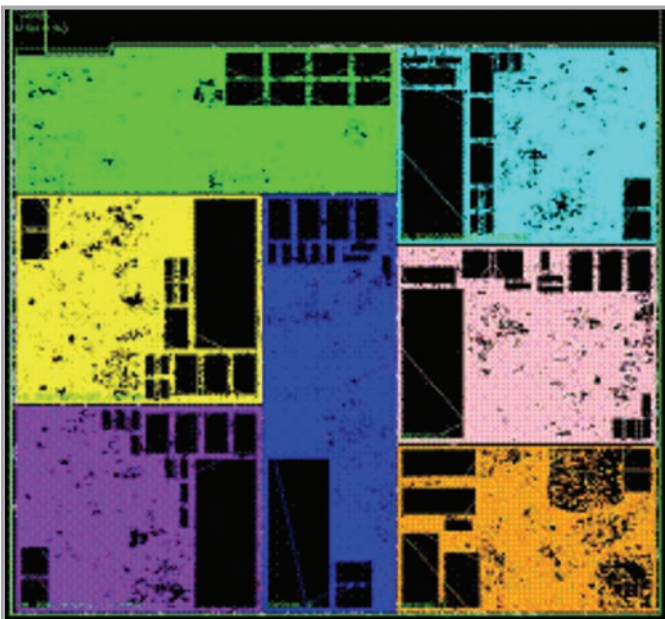
Unlike traditional flows that require the logic or physical designer to prepare a floorplan manually, Talus Design, prior to physical synthesis, can automatically generate a prototype-quality floorplan at the end of RTL synthesis. For prototyping purposes, this high quality floorplan is driven by virtually flat



*Automated non-uniform power-grid generation.*

placement of logic cells, timing- and congestion-driven macro placement, and various production-proven expert physical designer techniques captured in the automated decision process.

Unlike conventional synthesis tools, Talus Design does not waste time early in the flow performing optimizations based on estimated wire load models. As the physical knowledge of the design increases and more accurate data about global route and parasitics become available, additional optimizations such as cloning, restructuring and strength optimization are performed. These features produce designs that meet the target timing while minimizing area and power consumption. Conventional tools make these types of decisions too early in the logic synthesis step and ultimately inhibit the ability of the physical design tools to achieve design closure.



*Talus Design's congestion-aware macro placer.*

## Comprehensive and Configurable DFT Rule Check Engine

To improve testability of the design, Talus Design supports top-down and bottom-up hierarchical scan insertion throughout the synthesis and physical design flow. Talus Design has a comprehensive and configurable DFT flow check engine that allows the user to analyze and debug testability issues. A repair mechanism automatically adds test logic and optionally adds test points to resolve problems and help improve test coverage. During scan insertion, the scan chains are properly and safely balanced to help reduce test time. The chains can be verified with post scan flow checks, and the tool can quickly produce a fault coverage estimate within 1% of final results from commercial ATPG tools. Super-files for leading ATPG tools are automatically generated for a seamless handoff.

Additional DFT strategies such as on-chip test vector compression, logic BIST, memory BIST, and boundary scan insertion are supported in the form of RTL insertion as well as through interfaces to tools from leading DFT vendors. These interfaces are developed in collaboration with our MagmaTies DFT partners to help ensure a smooth integration of Talus Design and 3rd party DFT tools.

## Single Timing Analyzer and Constraints

Talus Design eliminates timing mismatches between synthesis and physical design using a single static timing analyzer throughout the RTL-to-GDSII flow. Design optimization constraints are set once at the RTL level and are used throughout synthesis and physical design. The optimization flow performs push-down operations on timing constraints for supporting top-down design flows, and pull-up operations for supporting hierarchical, IP- or black-box-based bottom-up design flows.

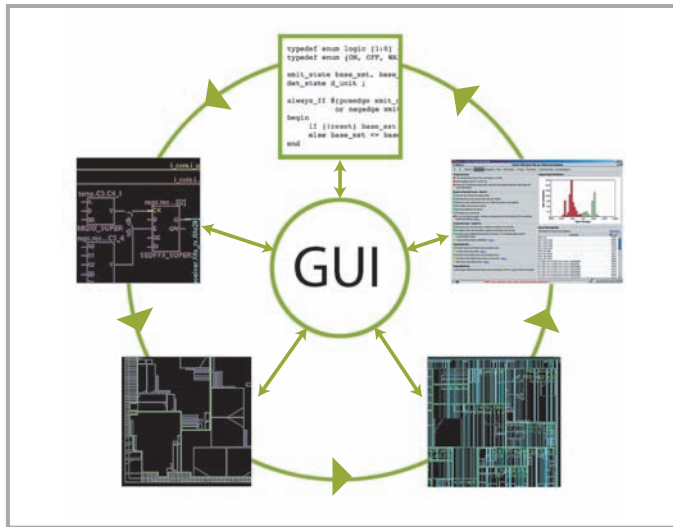
The constraints are set in widely adopted SDC format and support simultaneous multi-mode case analysis. Customized timing reports are available throughout the chip implementation flow. The built-in timer enables fast, incremental timing analysis following design changes during prototyping. Early insights into block- and chip-level timing help identify and fix potential timing problems from sub-optimal RTL code or incorrect design constraints in the early design stages.

The optional advanced timing and variability engines allow for concurrent, correct-by-construction timing results and optimizations across all modes and process, voltage and temperature (PVT) corners, while also considering both OCV and crosstalk effects. This implementation-level capability removes the need to iterate through a single-mode sign-off timer, greatly reducing turnaround time.

## Predictability Improves Productivity

Talus Design enables logic designers to experiment at early stages of the design process to improve RTL and timing constraints, allowing them to create a floorplan much earlier than in traditional flows. These early preparations can begin

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*Cross-probing accelerates quality improvement.*

with incomplete data. Details can be added as they become available, eliminating time-consuming iterations toward the end of the design cycle. This enables the logic designer to hand off the Volcano™ (Magma's binary data format) to the implementation team with a very high degree of confidence that it will achieve design closure. This ability to preserve all the known good aspects of a floorplan increases the predictability of the implementation and makes it easier to track, debug and modify the localized variations.

With the automated flow of Talus Design and Talus Vortex, implementation is no longer the bottleneck in the design process. Electronic System Level (ESL) designers can rapidly assess the impact of alternate system architectures on physical metrics such

as area, performance, power, routability, testability, manufacturability and yield. Any late-arriving specification, RTL or constraint changes can be easily accommodated without affecting the schedule or the productivity of the engineering team.

Talus also supports handoffs in industry-standard formats such as Verilog netlist, SDC constraints, UPF power intent and DEF placement for use with third-party physical design tools.

## Powerful GUI Speeds Design Debug and Exploration

Using the Talus Design schematic- or layout-based visualizations, logic designers can examine the functionality of RTL code and view logic levels, physical partitions, pin placement, clock distributions and timing paths throughout the flow. Cross-probing throughout the flow from the schematic, floorplan or layout into the RTL code allows logic designers to quickly identify, locate and fix problems due to timing constraints or improper RTL code structures. With this unique debug capability, designers can browse the logical hierarchy and guide partitioning decisions for floorplanning. Connectivity-driven visualizations such as fly-lines and clock-domain distribution provide valuable architecture and constraint improvement information. Slack-based timing histograms of critical paths in the built-in timing visualizer allow designers to quickly locate timing problems through direct cross-probing of RTL, schematic, floorplan or layout. Such analysis readily leads to identification of missing constraints or exceptions such as false paths or multi-cycle paths. Detailed power reports and maps provide power consumption and distribution information early in the design flow, saving back-end packaging and design re-spin costs.

### TECHNOLOGY FEATURES:

#### Full-Featured HDL Synthesis

- IEEE LRM-compliant Verilog, System Verilog and VHDL
- Incremental synthesis
- Dynamic data-path module generation
- Auto-pipelining and register retiming
- DFT scan checks, repair, insertion and optimization
- Distributed synthesis

#### Low-Power Optimization

- Hierarchical clock gating
- Integrated clock gate cells
- Automatic power-grid synthesis
- Support for Multi-Vt, Multi-VDD, MTCMOS libraries

#### Automated Macro and Standard Cell Placement

- Soft macro block shaping
- Macro placement and legalization
- Data-path architecture swapping during placement
- Comprehensive congestion analysis

#### Fast, Accurate Static Timing Analysis

- Hierarchical timing constraints
- Timing reports and graphical timing analyzer
- Multimode analysis

#### Advanced Features

- Logical and physical hierarchy management
- Flip-Chip pad ring synthesis
- Repeated blocks grouping in top-down flow
- High-capacity: large, complex, multimillion-gate designs

#### Inputs

- Verilog, System Verilog, VHDL, SDC, .lib, DEF, PDEF, UPF

#### Outputs

- Verilog, DEF, PDEF, SDC, SDF, SPEF, UPF

#### Platforms

- Linux, Sun Solaris



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