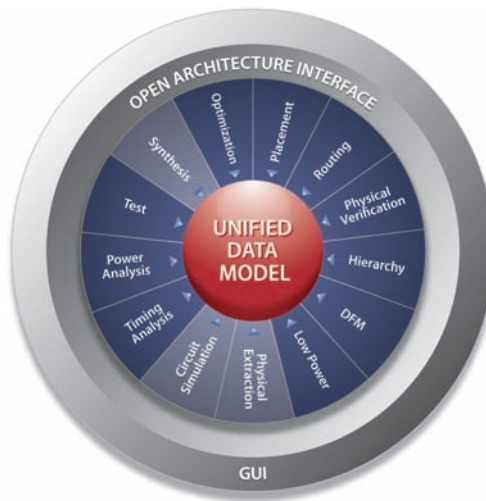


Talus[®] Vortex

- Fully automated congestion-aware macro-placer flow and optimization technology enable rapid exploration of the design space and provide a predictable path to design closure.
- Significant improvement in ROI due to 10 percent reduction in area, 5-10 percent improvement in performance or 30-50 percent reduction in power consumption.
- Unmatched timing and area results are enabled through an efficient delay model, integrated clock-tree technology, concurrent multi-mode and multi-corner analysis and optimization with integrated crosstalk prevention, and native on-chip variation (OCV) inclusion.
- Significant leakage reduction is achieved through an integrated implementation flow using multiple threshold voltage (multi-Vt) cells, without sacrificing performance.
- Embedded sign-off accuracy (with Quartz[™] RC and Quartz Time) for extraction, timing and noise eliminates post-layout analysis and repair iterations through third-party tools.
- Integrated design flow, single executable, common analysis engines and a unified data model enhance productivity, provide ease of use, eliminate unnecessary file transfers and ensure continuous correlation to final implementation.
- Proven 90-, 65- and 45-nm design support for major silicon vendors and foundries.

Talus Vortex is a physical design environment that enables rapid development of netlist- and chip-level constraints throughout the design process without sacrificing the quality of design or delivery schedule. This environment dramatically improves the productivity of physical designers by automating floorplan generation and complete design closure. This integrated implementation and sign-off system delivers improved timing and signal integrity, smaller area, lower power, better manufacturability, faster turnaround time and higher capacity than conventional point-tool flows. These capabilities, combined with optional automated distributed processing on multiple computers, enable Talus Design and Talus Vortex to implement any size design from RTL to GDSII in a predictable fashion.



Design engineers must make changes in the design specification throughout the implementation phase. In traditional hierarchical flows, once the RTL, timing and physical constraints are incorporated, substantial manual effort is required to propagate changes into the hierarchy, floorplan, size and shape of physical partitions and pad locations. For system-on-chip (SoC) designs at 65 nanometers (nm) and below, designers need an automated top-down or bottom-up full-chip synthesis methodology. Talus Vortex, in conjunction with Hydra[™], addresses all aspects of the design flow, eliminates time-consuming manual work, prevents the introduction of new errors – especially for changes that must be made late in the design phase – and ensures design closure.

The Talus Vortex implementation system provides a fully integrated netlist-to-GDSII flow for high-performance, high-complexity, low power nanometer designs that includes: optimization, placement, routing, useful skew clock generation, floorplanning and power planning, incremental RC extraction and a single incremental timing analysis engine. Built on Magma's unified data model and employing a new strength-based delay model, Talus Vortex sets a new standard for capacity, runtime and performance. In conjunction with the comprehensive low-power design capabilities of Talus Power, Talus Vortex provides significant power reductions without sacrificing timing and area.

Talus[®] Vortex

Strength-Based Delay Model for Optimal Timing

With Talus Vortex, Magma introduces optimization capabilities based on the new strength-based delay model. This new delay model accurately considers the effects of buffering and sizing at an early stage of optimization. Each cell is assigned a continuous drive strength that abstracts actual size available in the technology library. Rather than using fixed cells from a library, Talus Vortex replaces each logic function with automatically abstracted HyperCell™ models. These are functional placeholder cells with variable drive strength.

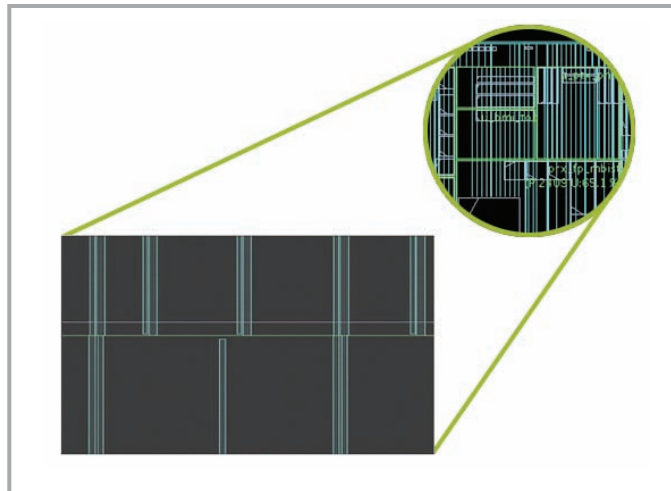
Initial placement and routing is done with the HyperCell model to determine the final optimal timing for all paths in the design. Layout optimization is performed by continuously adjusting the strength of each HyperCell as load and timing changes throughout the optimization process, allowing optimal delay to be achieved at any stage of optimization. Finally, the HyperCells are mapped to actual library cells with a discrete size. By employing optimal continuous sizing combined with adaptive buffering, Talus Vortex is able to deliver designs that consume less power and area while meeting timing requirements.

Built-in Low-Power Design and Optimization

Talus Vortex, with Talus Power as an option, provides an integrated power optimization flow, reducing power up to 20 percent over conventional standalone implementation tools while also delivering high performance. Power optimization capabilities deliver lower dynamic power consumption than conventional synthesis. Only optimal cell sizes are used to drive known loads, avoiding unnecessary power dissipation by cells. Balancing input slews to cells through optimal sizing is used to reduce total switching power. Additional power optimization capabilities such as multi-Vt library-based optimization, DFT-aware automatic clock gating, use of integrated clock gating cells in standard-cell library, detection of synchronously enabled registers and hierarchical insertion of clock-gating logic minimize power and improve testability.

Utilizing automatic power-grid synthesis for optimal power distribution, Talus Vortex, with Talus Power as an option, accepts user-defined power-grid constraints and automatically generates the appropriate power mesh. This method is extremely efficient in comparison to the spreadsheet approach that approximates power numbers based on legacy designs. Users can define utilization limits for each layer, current density or the voltage-drop limit as input constraints. Designers can also specify optimal parameters for the power grid and define pad locations during early planning, and then continue the refinement during detailed implementation. This eliminates the need to overdesign the power grid, saving precious routing resources and real estate on the chip. This automated method significantly reduces design closure time without sacrificing performance.

Advanced, low-power design capabilities are available as an option. These include voltage island support, automatic MTCMOS switch insertion and support for the Unified Power Format (UPF).

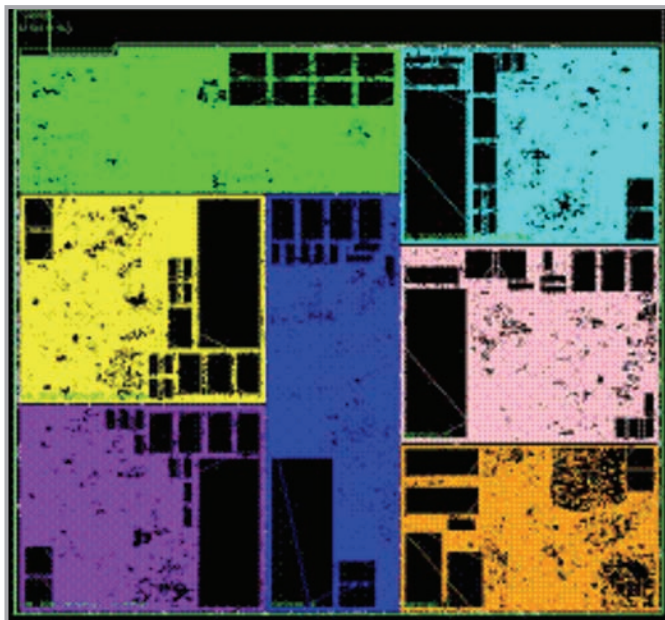


Automated non-uniform power-grid generation.

Automated Macro Placement and Physical Synthesis

Unlike traditional flows that require the logic or physical designer to prepare a floorplan manually, Talus Vortex can automatically generate a prototype quality floorplan at the end of RTL synthesis from an incoming netlist. For prototyping purposes, this high quality floorplan is driven by virtually flat placement of logic cells, timing- and congestion-driven macro placement, and various production-proven expert physical designer techniques captured in the automated decision process.

Unlike conventional synthesis tools, Talus Vortex does not waste time early in the flow performing optimizations based on estimated wire load models. As the physical knowledge of the design increases and more accurate data about global route and parasitics become available, additional optimizations such as cloning, restructuring and strength optimization are performed. These features produce designs that meet the target



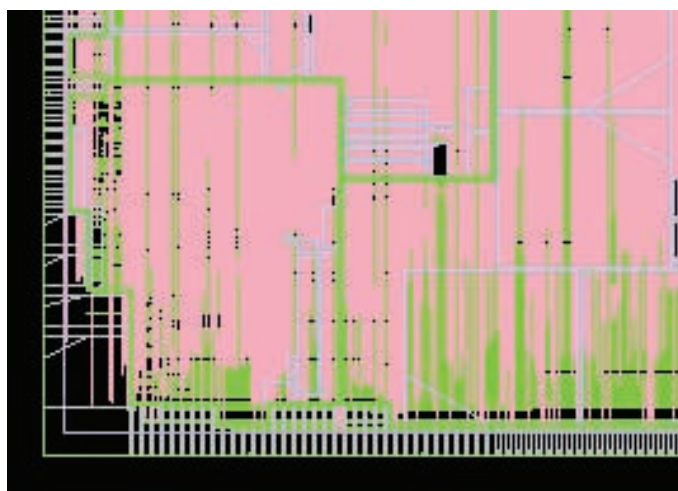
Talus Vortex's congestion-aware macro placer.

timing while minimizing area and power consumption. Conventional tools make these types of decisions too early in the logic synthesis step and ultimately inhibit the ability of the physical design tools to achieve design closure.

Block Implementation Delivers Unmatched Quality of Results

In typical benchmarks, Talus Vortex produces better timing and 5 to 10 percent smaller area than competitive solutions. Underlying the unmatched QoR are breakthrough block-level implementation technologies including:

The Embedded, Advanced Timing and Variability engines allow for concurrent correct-by-construction timing analysis and optimization across all modes and process, voltage and temperature (PVT) corners while also considering both OCV and crosstalk effects. Concurrently optimizing for complex multi-mode and multi-corner interactions during implementation eliminates the need to iterate through a single-mode sign-off timer, greatly reducing turnaround time.



Talus Vortex provides full top-level timing optimization including detailed route and automated re-assembly of all blocks.

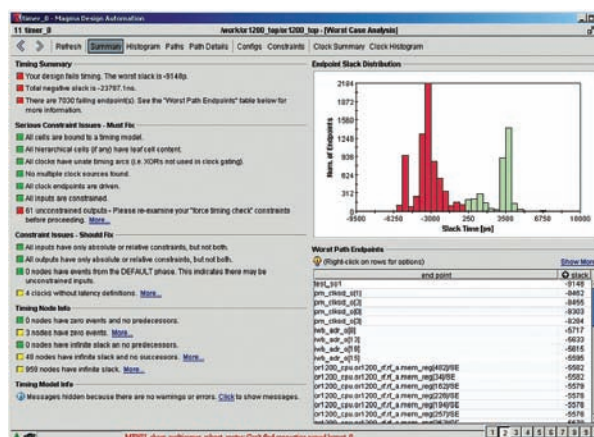
The Industry's Only Unified Data Model contains all the design data for a complete RTL-to-GDSII flow in a single data structure. This memory-resident data model enables the optimization, implementation and analysis engines to get immediate access to continuously updated logical, physical, timing and other design information. This allows the engines to make rapid and accurate on-the-fly design decisions that ensure optimal results.

Embedded Crosstalk Noise and Crosstalk Delay Engines enable Talus Vortex to address all crosstalk delay and crosstalk noise problems automatically and without iterations.

A Fast Implementation-Level Extraction Engine provides accuracy with slight pessimism, ensuring that the embedded sign-off extractor will detect only a minimal amount of new timing violations.

Clock Tree Synthesis is fully integrated to ensure that the clocks meet both timing and physical goals and also optimize for power with the Power option. Talus Vortex takes advantage of advanced techniques such as optimal clock-gate placement and cloning and un-cloning for better load distribution. It also leverages sophisticated clock algorithms that minimize skew while achieving timing requirements and maintaining design robustness under process variations and environmental differences. With the unique clock-tree visualization interface, users can browse, analyze and visualize the clock tree with ease.

The Next-Generation Router incorporates speed and rule improvements to deliver fast, DRC-clean routing. The timing- and crosstalk-driven router can perform top-level (hierarchical) as well as standard-cell routing. Its built-in polygon-based DRC engine provides clean routing and immediate feedback for advanced interactive routing. Talus Vortex fully supports 90-, 65- and 45-nm design rules from major silicon vendors and foundries, including complex spacing rules, common run-length rules, stacked-via rules and dense end-of-line rules. Talus Vortex automatically addresses complex antenna rules as well as other process-specific manufacturing requirements such as minimum area rules for vias, metal slotting and timing-driven metal fill. The integrated engines operating on the single data model allow for fast and accurate timing-driven wire spacing, metal fill for both grounded and floating metal, and native (not post-route) redundant via insertion. Talus Vortex provides the industry's best multithreading speedup for routing, and can be distributed across CPUs.

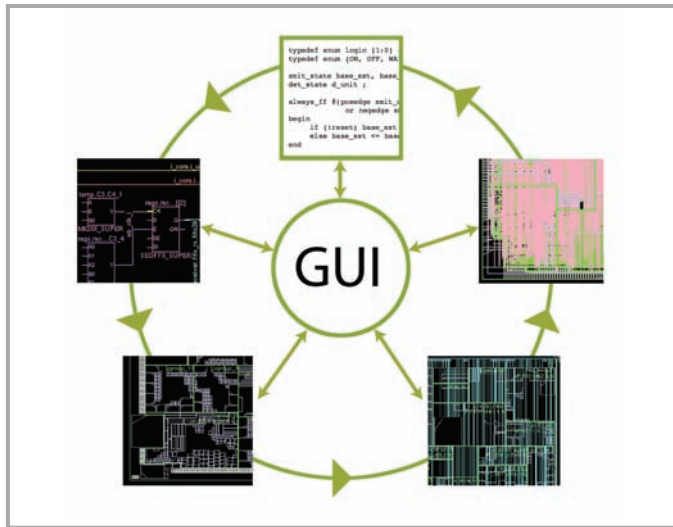


Talus Vortex's unique clock viewer allows users to browse, analyze and visualize the clock tree with ease.

Sign-off in the Loop

In conjunction with Quartz RC and Quartz Time, Talus Vortex provides advanced sign-off-level timing analysis and optimization capabilities. The embedded sign-off-accurate extraction, timing and noise analysis engines are used during design optimization, eliminating iterations between the implementation and sign-off flows. With the integrated Sign-off in the Loop™ technology, users can achieve complete timing closure faster than with conventional point-tool flows, reducing sign-off to a mere checklist activity.

Talus[®] Vortex



Cross-probing accelerates quality improvement.

The sign-off extraction accuracy is closely correlated to within 5 percent of the acknowledged industry gold standard for parasitic extraction, QuickCap[®]. Talus Vortex uniquely leverages Magma's QuickCap technology by using QuickCap CNE (Critical Net Extraction) for even greater accuracy on selected timing-critical nets. Talus Vortex offers additional advanced timing capabilities, such as enhanced current source model (ECSM) and composite current source (CCS) support.

Predictability Improves Productivity

With the automated flow of Talus Design and Talus Vortex, implementation is no longer the bottleneck in the design process. Electronic System Level (ESL) designers can rapidly assess the impact of alternate system architectures on physical metrics such as area, performance, power, routability, testability, manufacturability and yield. Any late-arriving specification, RTL, netlist or constraint changes can be easily accommodated without affecting the schedule or the productivity of the engineering team.

Powerful GUI Speeds Design Debug and Exploration

Using the powerful Talus Vortex visualization tool, designers can browse the logical hierarchy and guide partitioning decisions needed for floorplanning. Connectivity-driven visualizations such as fly-lines and clock-domain distribution provide valuable architecture and constraint improvement information. Slack-based timing histograms of critical paths in the built-in timing visualizer allow designers to quickly locate timing problems through direct cross-probing of RTL (with Talus Design), schematic, floorplan or layout. Such analysis readily leads to identification of missing constraints or exceptions such as false paths or multi-cycle paths. Detailed power reports and maps provide power consumption and distribution information early in the design flow, saving back-end packaging and design re-spin costs.

TECHNOLOGY FEATURES:

Nanometer Design Support

- Concurrent multi-mode/multi-corner analysis and timing optimization with embedded OCV and crosstalk
- Automated SPICE delay and crosstalk noise correlation
- Sign-off accuracy for extraction, timing and noise
- Embedded QuickCap Critical Net Extraction
- Emulated metal-fill extraction
- Current Source Models for timing

Low-Power/Low-Voltage Design Support

- Multi-Vt libraries support
- Embedded power analysis

Advanced Optimization Features

- Early useful-skew estimation
- Advanced timing visualization
- Incremental extraction, timing and noise

Advanced Placement Features

- High-capacity concurrent macro and cell placement
- Comprehensive congestion analysis

- Top-down and bottom-up I/O pin placement
- Scan chain reordering
- Multi-height cell placement with power/ground rail sharing

Advanced Clock Tree Features

- Useful/zero skew
- Low-power clock tree implementation using clock cloning/un-cloning and clock gates
- Inter-clock skew minimization
- Multiple clock domains
- Automatic gated-clock checks
- Clock tree viewer

Advanced Routing Features

- Virtual gridless router
- Interactive bus routing
- Complete ECO support
- 90/65/45-nm design and manufacturability rules
- Built-in polygon-based DRC engine
- Distributed and multi-threaded routing
- DFM-aware routing
- Crosstalk- and timing-driven

Crosstalk Noise Analysis

- DC and AC noise thresholds
- Accounts for multiple aggressors
- Timing window-based filtering
- Capacitance-based filtering
- Logical correlation filtering

Crosstalk Delay Analysis

- Timing window-based filtering
- Capacitance-based filtering
- Logical correlation filtering
- Slew-based crosstalk delay prevention
- Automatic timing window convergence

Input

- DEF (floorplan), Verilog (netlist), .lib, SDC, SPEF, LEF, GDSII, Volcano[™] (Magma format), UPF

Output

- DEF (floorplan), Verilog (netlist), .lib, SDC, SPEF/DSPF, LEF, GDSII, Volcano (Magma format), UPF

Platforms

- Linux, Sun Solaris



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