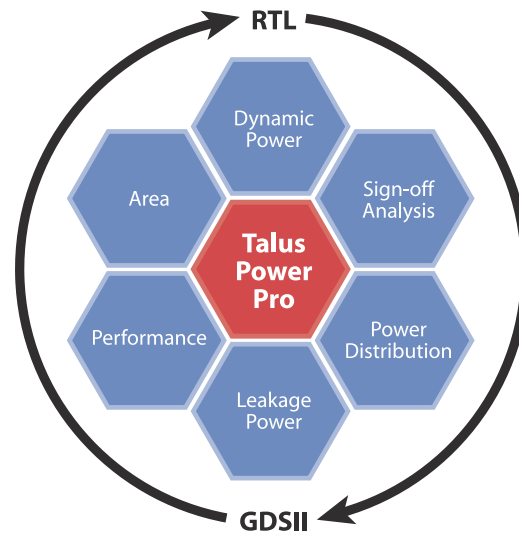


# Talus<sup>®</sup> Power Pro

- Provides a comprehensive solution for power optimization and management throughout the RTL-to-GDSII design flow.
- Addresses power early in the flow through power-aware synthesis that enables power gating, clock gating and other supporting techniques.
- Minimizes leakage power by using multi-threshold (multi-Vt) libraries.
- Supports an automated multi-Vdd methodology; allows definition of domains at the RTL stage, optimization and analysis across domains, and automatic insertion of level shifters and isolation cells.
- Power-aware clock tree synthesis ensures significant savings in power through advanced techniques such as sink clustering, clock gate cloning, un-cloning and optimal skew buffer insertion.
- Aggressively optimizes leakage power through MTCMOS insertion and analysis; supports distributed, global and standard-cell-specific variants.
- Automatically generates power grids based on specified constraints through automatic power grid synthesis.
- Minimizes leakage power and improves yield through automatic optimization and insertion of decap cells based on transient analysis.
- Minimizes switching power and ensures uniform power and voltage-drop distribution through advanced power-aware buffering and sizing.
- Enables continuous power, timing and area tradeoffs throughout the RTL-to-GDSII flow with unified data model architecture and embedded analysis engines.
- Supports both Common Power Format (CPF) and Unified Power Format (UPF) industry standards for low power to significantly improve turnaround time and interoperability.

Talus Power Pro, a key component of Magma's integrated IC implementation platform, provides a comprehensive RTL-to-GDSII solution for power optimization and management. Talus Power Pro enables optimal power management throughout the flow with power-aware synthesis, physical optimization, clock tree synthesis and routing, allowing designers to minimize power and ensure uniform power distribution. Talus Power Pro is fully integrated with Magma's implementation flow to provide continuous power, timing and area tradeoffs throughout the design flow.



The increasing use of battery-powered portable electronic systems is driving the demand for digital integrated circuits (ICs) that consume the smallest possible amount of power. At the same time, designers must pack more functionality onto chips that operate at very high frequencies, while minimizing the package size. Increasing performance and cell count result in increased power, making power management critical to silicon success.

To achieve optimal results without increasing turnaround time, continuous, on-the-fly tradeoffs between power and timing have to be made throughout the RTL-to-GDSII flow. Traditional approaches to power management require multiple tools and use of custom techniques. This lack of integration makes it impossible for point-tool flows to adequately address power and other design requirements. Talus Power Pro offers a comprehensive low-power solution that is fully integrated into Magma's RTL-to-GDSII flow. Talus Power Pro enables efficient power management throughout the flow, ensuring rapid convergence. It also leverages embedded power, timing and voltage (IR) drop analysis engines to enable tradeoffs without having to leave the implementation system.

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## Power-Aware Synthesis Addresses Power Early in the Design Flow

Addressing power very early in the flow ensures good quality of results (QoR) and minimizes iterations for faster turnaround time. Talus Power Pro is tightly integrated with Magma's IC implementation flow to enable concurrent power, timing and area optimization during synthesis. It provides dynamic power savings by using clock gating techniques that also include support for test logic. At the same time, Talus Power Pro enables dynamic power reduction by recognizing special directives in the RTL to insert power gating cells and retention flip-flops.

## Leakage Power Minimization Using Multi-Vt Libraries

By using multi-Vt libraries, Talus Power Pro maximizes leakage power reduction. Cells from the different libraries are combined into a single library and then the best cells are automatically selected to satisfy both timing and leakage power requirements. The optimization engine makes leakage-power-versus-timing tradeoffs at multiple stages of the implementation flow and minimizes the number of low Vt (faster, but higher leakage) cells required in the design.

## MTCMOS Switch Insertion and Analysis Significantly Minimizes Leakage Power

Multi-threshold CMOS (MTCMOS) switches are used to connect the global constant power rails to the local switched power rails. These switches effectively allow certain blocks in the design to be powered off depending on the chip's mode of operation, reducing leakage power up to 10x. Magma's methodology supports insertion and sizing of different types of MTCMOS switches such as global header/footer switches, distributed or fine-grain header and footer switches and standard-cell-based switches. Incremental insertion and enable-line stitching are handled automatically. The transient IR-drop capability can be used to analyze power on/off times for the MTCMOS regions.

## Automated Methodology Supports Designs with Voltage Islands

Voltage islands provide the flexibility to reduce power by selectively shutting down different regions or running islands at different voltages. Talus Power Pro provides a complete automated methodology for designs containing different voltage islands. This automated methodology

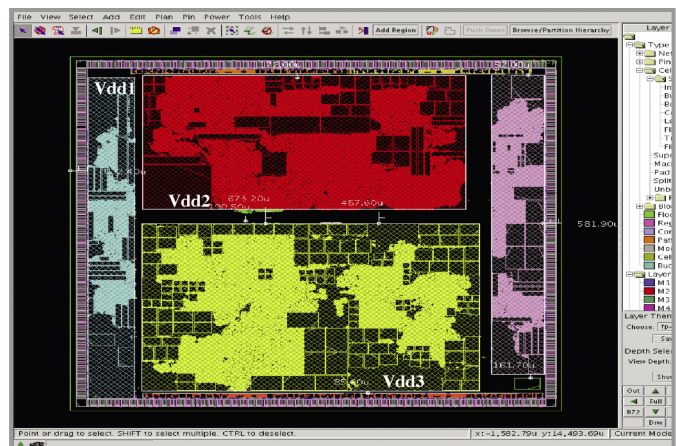
supports both the hierarchical flow and a virtually flat flow that provides better QoR. Based on user specifications, Talus Power Pro automatically creates voltage islands, connects the power and ground nets, and inserts and places special cells such as level shifters and isolation cells. Talus Power Pro can optimize within each of these voltage domains using the appropriate cells from the corresponding libraries. Talus Power Pro also enables dynamic voltage versus frequency scaling (DVFS) by performing concurrent multicorner timing optimization for the different operating conditions. Talus Power Pro also supports RTL pragmas to define voltage domains during synthesis.

## Power-Aware Clock Tree Synthesis Helps Optimize Clock Tree Power

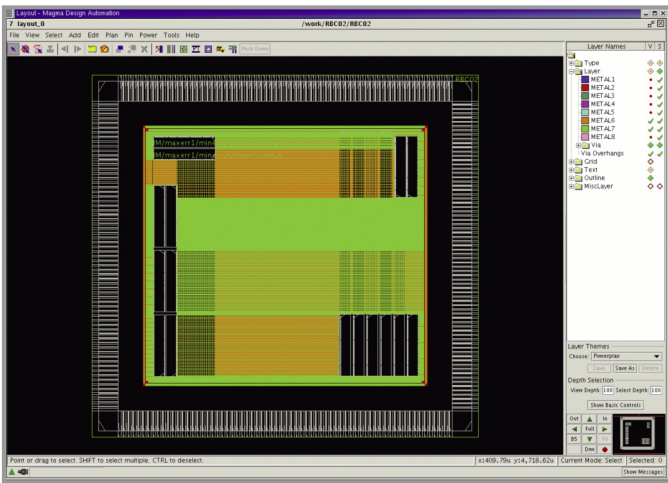
Power consumed in the clock tree constitutes a significant portion of the total chip power. Talus Power Pro employs a variety of techniques to optimize clock tree power during clock tree synthesis. Advanced techniques (such as netlist-level clock gating, physically-aware cloning and uncloning of clock gates, multi-Vt, power-aware buffering, sizing and sink clustering) are employed during clock tree construction. Power and timing are both considered as cost functions for optimal QoR. Additional techniques such as activity-driven clock gating and clock tree balancing help further optimize clock tree power.

## Automatic Power-Grid Synthesis for Optimal Power Distribution

Talus Power Pro accepts user-defined power-grid constraints and automatically generates the appropriate power mesh. This method is extremely efficient in comparison to the spreadsheet approach that approximates power numbers



*Talus Power Pro's virtually flat automated voltage island methodology enables optimization and analysis across domains.*



*Power-grid synthesis automatically generates power grids based on user-specified constraints.*

based on legacy designs. Users can define utilization limits for each layer, current density or the voltage-drop limit as input constraints. Designers can also specify optimal parameters for the power grid and define pad locations during early planning, and then continue the refinement during detailed implementation. This eliminates the need to overdesign the power grid, saving precious routing resources and real estate on the chip. This automated method significantly reduces design closure time without sacrificing performance.

### Automatic Optimization and Insertion of Decap Cells Based on Transient Analysis

Tightly integrated with Talus Power Pro, Magma's Quartz™ Rail provides accurate transient rail analysis, allowing Talus Power Pro to automatically perform decoupling capacitance insertion and optimization, minimizing power network fluctuations due to these transient effects. Intelligent insertion ensures minimum leakage power consumption on the decap cells, improves reliability and minimizes power distribution noise.

### CPF and UPF Support for Low-Power Designs

Talus Power Pro utilizes either CPF or UPF at the beginning of the RTL-to-GDSII flow to read in the power constraints for the low-power flow. Power constraints such as clock gating, retention-flop synthesis and multi-Vdd domain definitions can be defined for dynamic power reduction. Special cells such as level shifters and isolation cells can be inferred during the synthesis stage to support multi-Vdd flows. For domains that are powered down, switches can be inferred at the

RTL state to facilitate simulation. State tables can be used to define the relationship between the different domains that have been created. Talus Power Pro can also write out either CPF or UPF at any point in the design flow for easy interoperability.

### Low-Power Reference Methodology Supports Use of Special Library Cells and IP

Talus Power Pro provides a complete power management platform by supporting reference methodologies from foundries, library vendors and custom intellectual property (IP) vendors. Third-party vendors have various programs to help customer-owned tooling (COT) designers build low-power applications. The basic architecture to support dynamic and leakage power reduction scales across standard cells, I/Os, memories and analog IP blocks. Special cells such as level shifters, retention flip-flops, isolation cells and MTCMOS cells are supported in Talus Power Pro. The views for these cells are available to help in the low-power implementation process. This modular approach helps users mix and match elements in their design flow for optimal power reduction. Decoupling capacitance characterization on standard cells can be done once the SPICE models are provided.

#### TECHNOLOGY FEATURES:

##### Dynamic Power

- Completely automated, virtually flat multi-Vdd flow
- Dynamic voltage versus frequency scaling (DVFS)
- Power-aware synthesis and physical optimization
- Clock-gate insertion

##### Leakage Power

- Leakage power minimization using multi-Vt libraries
- MTCMOS and VTCMOS (body bias) techniques to reduce leakage power

##### Power Distribution

- Power and IR-drop analysis
- Automatic power-grid synthesis
- Intelligent decoupling capacitance optimization based on transient analysis

##### Supports CPF and UPF and Provides Reference Methodology

- Supports both CPF and UPF low-power industry standards
- Reference methodology to utilize special library cells and custom IP
- Accurate characterization of models that ensures predictability of silicon

##### Tight Talus Platform Integration

- Ideal sizing during optimization minimizes power consumption
- Built-in power router
- Power and IR-drop analysis
- Setup and hold time fixes due to IR drop

MAGMA DESIGN AUTOMATION

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