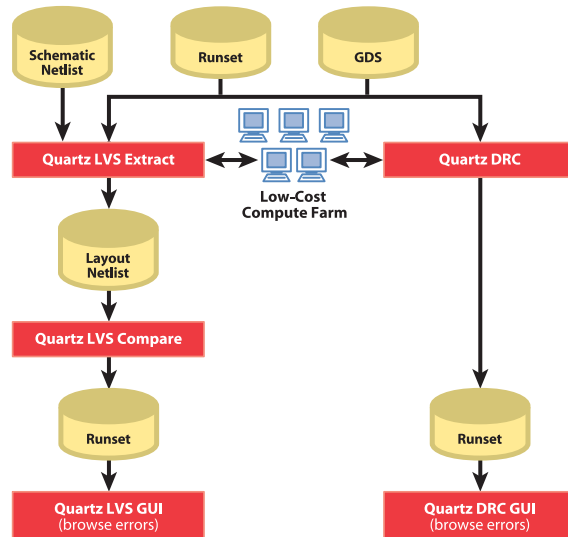


Quartz™ DRC and Quartz LVS

- Fully scalable architecture allows any design to run in 2 hours or less, regardless of design size or technology node.
- Memory-controlled architecture typically uses less than 2 gigabytes (GB) of memory, enabling affordable distributed computing on low-cost Linux machines.
- Tcl runset language and graphical run set debugger provide programming power and unmatched productivity.
- Built-in, advanced DFM modeling of lithography effects ensures higher accuracy and provides a complete lithography-friendly design flow to reduce parametric and catastrophic yield loss.
- Key productivity improvements provide for density, fill, antenna checking, rule-based yield scoring and short-finding utilities – reducing day-long or week-long tasks to hours or minutes.
- Native integration with Blast Fusion® allows for in-the-loop incremental DRC, speeding time to tapeout – greatly improving design productivity.
- Proven at major foundries worldwide with fully qualified runsets available.

Quartz DRC and Quartz LVS are the industry's first fully scalable physical verification solutions. Leveraging a unique architecture and advanced modeling capabilities, these revolutionary products allow affordable massively distributed processing of DRC and LVS comparison and integrate inherent DFM knowledge into the physical verification. With this technology and the right number of processors, virtually any design can be physically verified in 2 hours.



At 90 nanometer (nm) and below, there is a sharp increase in the size of designs and the complexity of design rules. These issues become even more severe at 65 nm, as manufacturability concerns, primarily lithography effects, are no longer just a problem for the fab, but something that every designer must consider. As a result, traditional physical verification architectures are no longer sufficient to address the performance and design for manufacturability (DFM) demands of today.

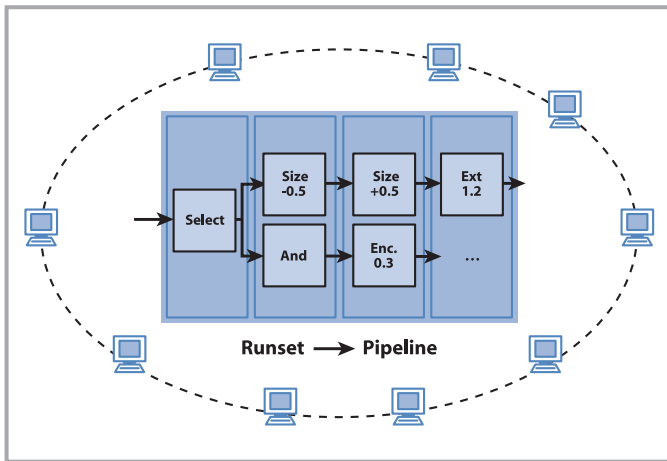
Quartz DRC and Quartz LVS are revolutionary new tools architected around two major premises. Designs at 90 nm and below need to have a scalable solution that makes effective use of available Linux compute farms to overcome the increases in design size and complexity of today's designs. Also, designers need to be able to take lithography effects into account while performing physical verification. Quartz DRC and Quartz LVS were designed with these two requirements in mind.

Quartz DRC and Quartz LVS

Pipelining Breaks the Scalability Barrier

In Quartz DRC and Quartz LVS, a pipelined architecture utilizes grid-computing and multicore architectures to perform massively distributed processing, improving both turnaround time and capacity by more than 10x.

Using this architecture, the physical verification problem can be split into smaller, independent tasks, making it easy to keep a farm of Linux machines busy. This enables linear acceleration as the number of CPUs increases, allowing a design team to specify the desired turnaround time for physical verification in the design cycle.

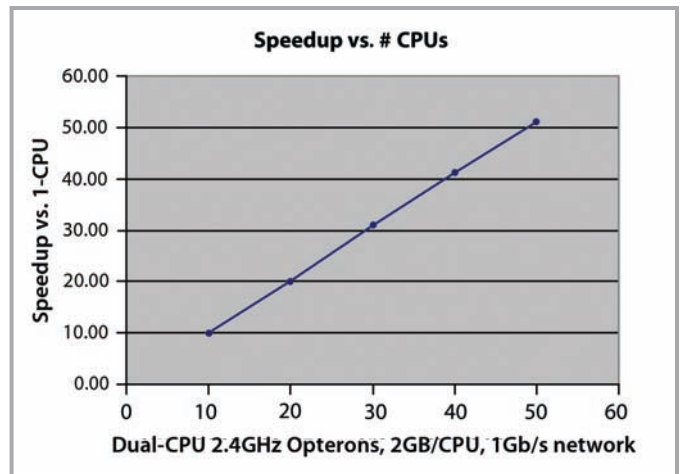


The pipelined architecture enables massively distributed processing, which improves both turnaround time and capacity by more than 10x.

Affordable Computing With Memory-Controlled Architecture

Traditional physical verification tools can only make effective use of four, or at most eight, CPUs for DRC; and that number is even lower for LVS and connect-based operations. They also require a tremendous amount of shared RAM to service the hierarchical requests from the CPUs. As a result of growing design sizes, the cycle time for physical verification has consistently increased and so has the need to use more expensive computers.

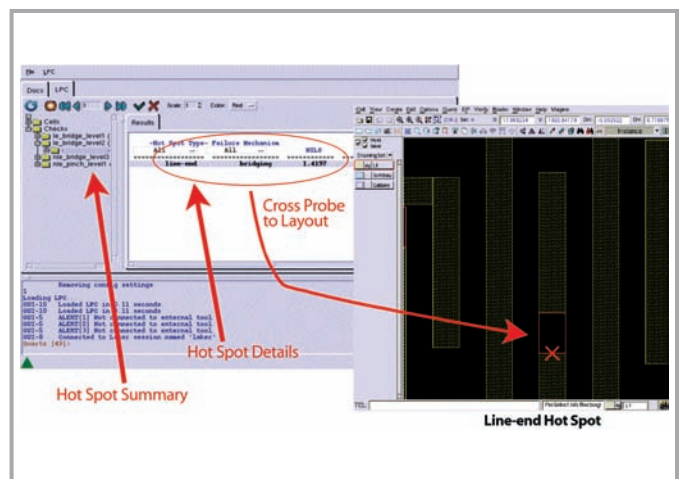
With its ability to break the physical verification process into many smaller tasks, Quartz DRC and Quartz LVS can efficiently and effectively run on very low-cost computers. For example, a 10 GB GDSII file can be run on 40 CPUs in less than two hours, and the peak memory usage is about 1.0 GB. This example illustrates the speed and capacity improvements, but does not define the limits of the Magma technology. Speed and capacity scales to larger GDSII files and large CPU farms.



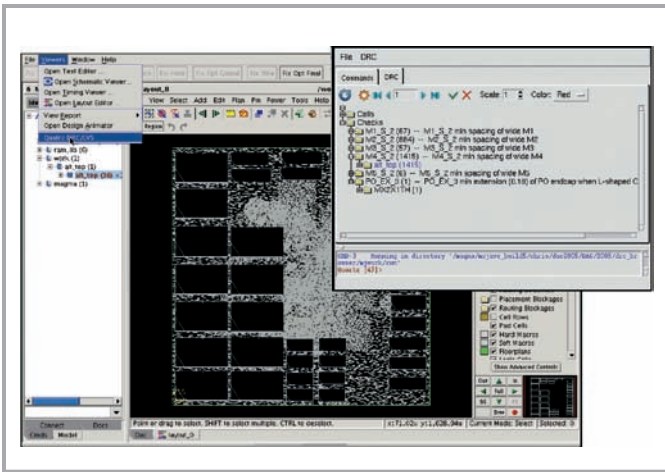
Physical verification accelerates linearly as the number of CPUs increases.

Advanced, Built-In DFM Modeling Ensures Accuracy

Unlike traditional physical verification products, Quartz DRC was architected with DFM and lithography issues in mind. Layout patterns might be DRC clean, but at 65 nm they result in bridging, pinching or other lithography issues that will result in catastrophic or parametric yield problems. This problem can no longer just be understood and addressed at the fab, but must be considered throughout the design flow. Quartz DRC provides a full lithography simulation for real model-based design verification. This lithography simulation is used to perform lithography process checks (LPCs) and identify potential lithography hot spots, as well as to guide the physical design phase in the Magma Blast Fusion and Talus™ design implementation products.



Lithography simulation is used to perform lithography process checks (LPCs), identify potential lithography hot spots and guide physical design.



Quartz DRC and Quartz LVS error browsing is completely integrated into the Blast Fusion and Talus implementation environments.

Quartz DRC and Quartz LVS provide other unique features for DFM. The architecture naturally facilitates accurate chemical mechanical polishing (CMP) checking in only a fraction of the runtime of other tools. Severity reporting for DFM violations and design scoring provide access to full-chip statistical analysis of manufacturability problems.

Increased Productivity With Tcl Programmable Input

Quartz DRC and Quartz LVS are the first physical verification products with an open Tcl interface and provide unparalleled ease of use and functionality. Using Tcl scripts designers can program the input, runset and output. These fully programmable runsets are small, easy to read and easy to maintain.

The database of results is also fully accessible through Tcl. Quartz DRC and Quartz LVS commands that access that database are provided in Tcl code, allowing designers to modify or enhance the commands. For example, all DRC error reporting is done through Tcl routines that can be easily configured to support any output format. This capability makes it easy to integrate Quartz DRC and Quartz LVS into existing flows.

Seamless Integration With Blast Fusion and Talus

Quartz DRC and Quartz LVS are fully integrated into the Magma design implementation tools. In a single command, designers can invoke Quartz DRC and Quartz LVS from within the design environment. The Volcano™ database is read and merged with reference library GDSII files, and then the results are imported back into the design environment for viewing and fixing.

This flow can be used for in-the-loop verification during the design phase, and includes an incremental capability for even faster turnaround time.

Complete Debug Environment

The DRC, LVS and LPC GUIs provide a full suite of error browsing capabilities. The GUIs are fully integrated into the Magma Blast Fusion physical design system and the Virtuoso and Laker layout editors. Errors can be organized by cell or by error type and can be marked as either fixed or ignored.

The short-finding capabilities within Quartz DRC and Quartz LVS are built on a unique approach that provides very fast and accurate diagnosis of the location of the short circuit. Multiple short circuits can be found in a single run and the results are immediately available within the GUI environment.

The LVS GUI has many unique capabilities that provide ease of use and speedy debugging. All LVS results are organized and presented to guide the designer to a quick and intuitive understanding of the results and the best method to begin fixing any errors. The GUI can render any portion of the layout or schematic as a schematic making it faster and easier to visualize connectivity differences and pinpoint areas that need detailed analysis.

TECHNOLOGY FEATURES

- Full set of geometric processing capabilities based on the pipelined architecture
- Built-in model-based lithography simulation
- All reporting done through user-visible Tcl routines for easy customization
- Single GUI for DRC, LVS and LPC with full interface to Blast Fusion, Virtuoso and Laker
- Integrated execution from within the Blast Fusion and Talus design environments
- Direct support for foundry runsets
- Supports LSF and "rcommand" job distribution

Inputs

- Layout: GDSII, OASIS, Volcano
- Netlist: Verilog or SPICE
- Runset and extension language: Tcl

Outputs

- GDSII, SPICE and Tcl accessible cross-reference database

Platforms

- Linux
- AIX

MAGMA DESIGN AUTOMATION

Quartz DRC and Quartz LVS



1650 Technology Drive, San Jose, CA 95110 USA | Tel: 408-565-7500 | Fax: 408-565-7501 | www.magma-da.com

© 2006 Magma Design Automation, Inc. All rights reserved. Magma and Blast Fusion are registered trademarks and Quartz, Talus and Volcano are trademarks of Magma Design Automation. All other product and company names are trademarks or registered trademarks of their respective companies. 07/06

